REMARKS

In response to the Office Action of September 28, 2004, Applicants respectfully request reconsideration. Claims 1-9 were previously pending in this application. Claim 1 has been amended. New claims 10-19 have been added. As a result, claims 1-19 are pending for examination, with claims 1,10 and 15 being independent. No new matter has been added.

Rejections Under 35 U.S.C. §102

The Office Action has rejected claims 1, 2, 4, and 6-9 under 35 U.S.C. §102 as purportedly being anticipated by Abadeer. Claim 1 has been amended to clearly distinguish over Abadeer.

Abadeer discloses a programmable storage element which includes a plurality of first resistors and a switching circuit for coupling the first resistors in series in response to a plurality of first control signals. The switching circuit also couples the first resistors in parallel in response to a plurality of second control signals to permit programming of the first resistors (abstract). The device disclosed by Abadeer in figure 3 (relied upon in the Office Action) contains four transistors Q_{fa} - Q_{fd} receiving a plurality of control signals at control terminals T_a - T_d respectively (Col. 7, lines 8-10). Resistors F_{1A}, F_{1B} and F_{1C} are connected in series between a supply voltage source V_{dd} and an output terminal T (Col. 7, lines 20-22).

Claims 1, 2, 4 and 6-9:

As amended, claim 1 is directed to a resistive element controllable to irreversibly decrease its value, comprising several polysilicon resistors connected in series between two input/output terminals of the resistive element and an assembly of switches connected to turn the series connection into a parallel association of said resistors between two programming terminals, the two programming terminals being different from the input/output terminals, intended to receive a supply voltage.

The Office Action asserts that Abadeer teaches resistors connected in a parallel association between two programming terminals T_b and T_d intended to receive a supply voltage V_{dd}. Applicants respectfully disagree. Terminals T_b and T_d do not receive a supply voltage, but instead only receive a control signal. Abadeer does not teach two programming terminals, the

two programming terminals being different from the input/output terminals, which receive a supply voltage, as recited in amended claim 1. Therefore, claim 1 patentable distinguishes over Abadeer and the rejection under §102 is improper and should be withdrawn. Claims 2-9 depend from claim 1 and are patentable for at least the same reasons.

Newly Added Claims

New independent claims 10 and 15 correspond, respectively, to previously pending claims 3 and 5 rewritten in independent form. Claims 3 and 5 were rejected under 35 U.S.C. §103 as purportedly being obvious over Abadeer in view of O'Shaughnessy. Applicants respectfully disagree.

O'Shaughnessy discloses a clock overdrive function which is said to allow precise control of circuit timing (abstract). In figure 2 (relied upon in the Office Action), O'Shaughnessy discloses a transistor level schematic drawing of a self-calibrating RC oscillator circuit comprised of seven N-channel transistors and eleven P-channel transistors.

a. Claims 10-14

Claim 10 is directed to a resistive element controllable to irreversibly decrease its value, comprising several polysilicon resistors connected in series between two input/output terminals of the resistive element, and an assembly of switches connected to turn the series connection into a parallel association of said resistors between two programming terminals intended to receive a supply voltage. The assembly of switches comprises one more switch than the resistive element comprising resistors, with one of the switches connecting one of said input/output terminals to one of said programming terminals. The assembly of switches further comprises MOS transistors with a number of N-channel transistors greater by one than the number of P-channel transistors.

The Office Action concedes that Abadeer does not teach a switch assembly comprising MOS transistors with N-channel transistors and P-channel transistors, whereby the number of N-channel transistors is equal to or greater by one than the number of P-channel transistors, but asserts that O'Shaughnessy teaches the use of N-channel transistors which are equal to or greater

by one than the number of P-channel transistors so as to provide a better control of circuit timing. Applicants respectfully disagree.

O'Shaughnessy does not specifically state or teach that the use of a number of P-channel transistors equal to or greater than the number of N-channel transistors improves the control of circuit timing. Thus, the alleged motivation for the modification to Abadeer is unsupported. In addition, even if one skilled in the art would have been motivated to combine Abadeer and O'Shaughnessy for the purpose of achieving precise control of circuit timing, which Applicant does not concede, the resulting device would include the device featured in Abadeer with an external self-calibrating RC oscillator circuit as taught by O'Shaughnessy. There is simply nothing in the prior art of record that would have motivated one to modify the device of Abadeer so that the number of transistors of a P-channel type are equal to or greater than those of N-channel type, which is a requirement of claim 10. In view of the forgoing, it is respectfully asserted that claim 10 patentably distinguishes over the prior art of record. Claims 11-14 depend from claim 10 and are patentable for at least the same reasons.

b. Claims 15-19

Claim 15 is directed to a resistive element controllable to irreversibly decrease its value, comprising several polysilicon resistors connected in series between two input/output terminals of the resistive element, and an assembly of switches connected to turn the series connection into a parallel association of said resistors between two programming terminals intended to receive a supply voltage. The switch assembly comprises as many switches as the resistive element comprises resistors, with one of said input/output terminals being the same as one of said programming resistors. The switches are formed of MOS transistors distributed half and half between P-channel and N-channel transistors.

As should be appreciated from the discussion above relating to claim 10, O'Shaughnessy does not specifically state or teach that the use of a number of P-channel transistors equal to or greater than the number of N-channel transistors improves the control of circuit timing. Thus, the alleged motivation for the modification to Abadeer is unsupported. In addition, there is simply nothing in the prior art of record that would have motivated one to modify the device of Abadeer so that the number of transistors of a P-channel type are equal to or greater than those of N-channel type, which is a requirement of claim 15. In view of the forgoing, it is respectfully

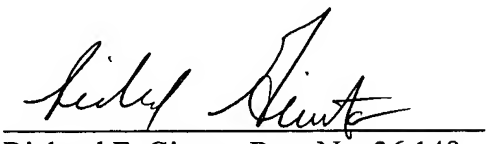
asserted that claim 15 patentably distinguishes over the prior art of record. Claims 16-19 depend from claim 15 and are patentable for at least the same reasons.

CONCLUSION

In view of the foregoing, the application is believed to be in condition for allowance. A notice to this effect is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Michel Bardouillet et al., Applicants

By: 

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